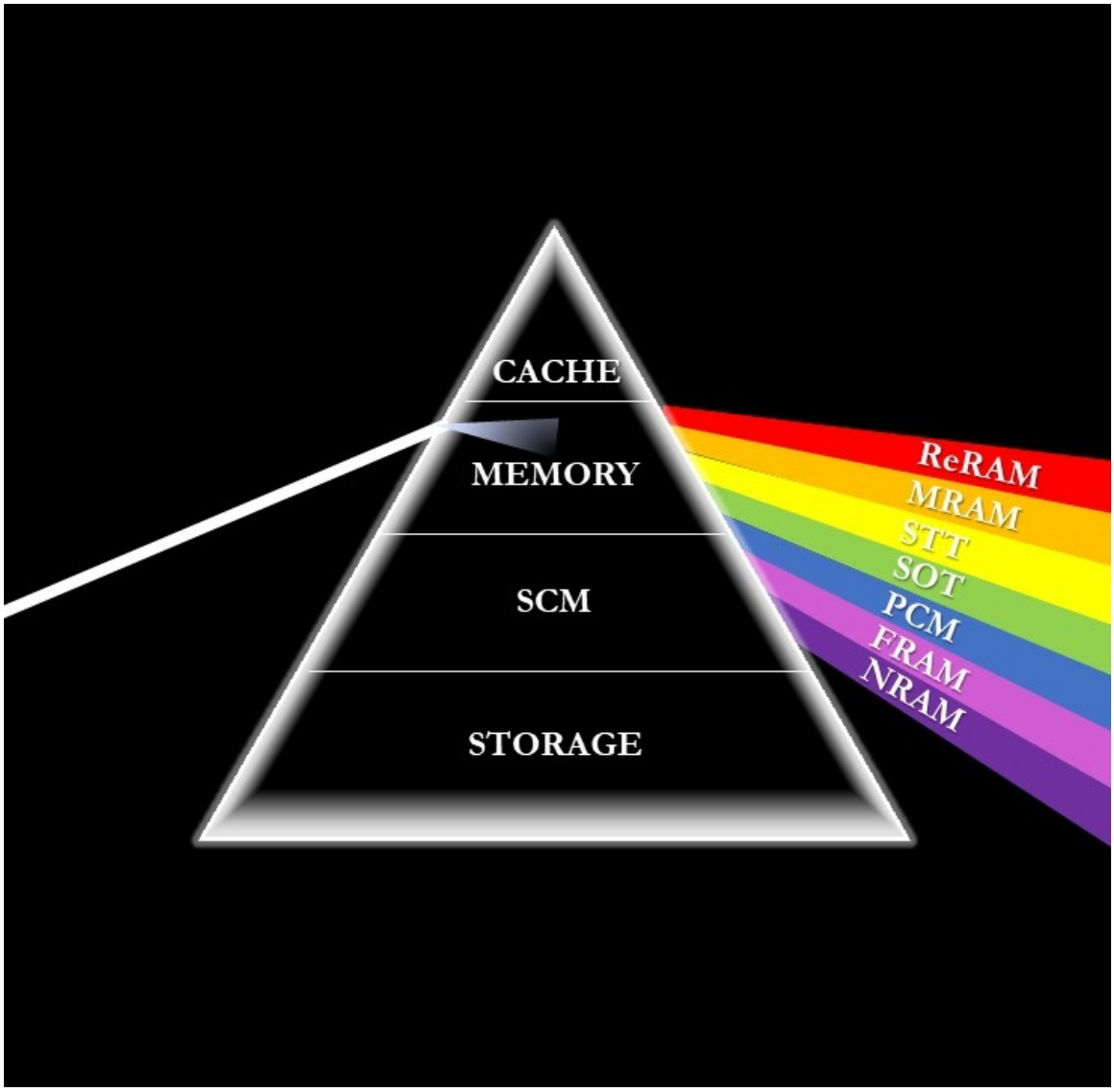
EMERGING MEMORIES ENTER THE NEXT PHASE



COUGHLIN ASSOCIATES & OBJECTIVE ANALYSIS

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EXECUTIVE SUMMARY

Flash memory (NAND and NOR), DRAM, SRAM, and other popular memory technologies are facing potential technology limits to their continued improvement. This has resulted in intense efforts to develop new memory technologies. Most of these new technologies are nonvolatile memories, which can be used for long-term storage or to provide a memory that retains information when powered down. Nonvolatile memories offer advantages for battery and ambient powered devices and also for energy savings in data centers.

PCM, ReRAM, FRAM, Toggle MRAM, and STT MRAM are emerging memories addressed in this report, as well as a variety of less mainstream technologies such as carbon nanotubes. Based upon the level of current development and the characteristics of resistive RAM (ReRAM) technologies, they may be a potential replacement for flash memory. However, NAND flash memory will continue to undergo several generations of improvement that will be implemented before a replacement is required. A transition from NAND flash to some other technology will likely not occur until the next decade, at the earliest.

Since last year's report we have learned that the economies of scale play perhaps an even larger role in the emerging memories market than we already thought. Micron has exited the 3D XPoint market and Intel has seriously trimmed its Optane product offerings, while outright disclosing the losses attributable to this technology, which were in line with Objective Analysis estimates. More recently, on July 28, 2022, Intel said that it was "Winding Down" its Optane memory business. Since this edition was already close to publication when Intel's announcement was made, our forecasts do not yet reflect this change. We plan to issue an update to the report in the near future, taking into account Intel's announcement. Report purchasers will be provided this update without charge once it is published.

Magnetic RAM (MRAM) and spin transfer torque RAM (STT MRAM) are starting to replace some NOR flash and SRAM and could possibly displace some DRAM within the next few years, probably before ReRAM replaces NAND flash memory. The rate of development and increasing product volume in STT MRAM and other MRAM technologies will gradually result in lower prices. The attractiveness of replacing volatile memory with high speed and high endurance nonvolatile memory make these technologies very competitive, assuming that their volume increases to reduce production costs (and thus purchase prices).

Ferroelectric RAM (FRAM) and some ReRAM technologies have some niche applications and with the use of HfO FRAM the number of niche markets available for FRAM could increase.

Moving to a nonvolatile solid-state main memory and cache memory will reduce power usage directly as well as enable new power saving modes, provide faster recovery from power off and enable more stable computer architectures that retain their state even when power is off. Eventually spintronic technology, that uses spin rather than current

for logic functions, could be used to make future microprocessors. Spin-based logic could enable very efficient in-memory computing. Several emerging memory technologies are also being used in neuromorphic computing experiments.

The use of a nonvolatile technology as an embedded memory combined with CMOS logic has great importance in the electronics industry. NOR flash reached its scaling limit at 28nm, and is being replaced with one of these new non-volatile technologies (especially MRAM and ReRAM). As a replacement for a multi-transistor SRAM, STT MRAM could dramatically reduce the number of memory transistors and thus provide a low cost, higher-density solution. A number of enterprise and consumer devices use MRAM, to act as an embedded cache memory, and this trend will continue.

Because of the compatibility of MRAM and STT-RAM processes with conventional CMOS processes, these memories can be built directly on top of CMOS logic wafers. Flash memory doesn't have the same compatibility with conventional CMOS. The power savings of nonvolatile and simpler Toggle MRAM and STT MRAM when compared with SRAM is significant. As MRAM $/GB costs approach those of SRAM, this replacement could cause significant market expansion.

It is projected that total MRAM and STT MRAM baseline annual shipping capacity will rise from an estimated 34.8TB in 2021 to 2.14EB in 2032. Total MRAM and STT-RAM baseline revenues are expected to increase from $91M in 2021 to about $43.6B by 2032.

Much of this revenue gain will be at the expense of SRAM, NOR flash and some DRAM, although STT-RAM is developing its own special place in the pantheon of shipping memory technologies.

The demand for MRAM and STT-MRAM will drive demand for capital equipment to manufacture these devices. While MRAM and STT-MRAM can be built on standard CMOS circuits supplied by large semiconductor fabricators, MRAM and STT MRAM do require specialized fabrication equipment for the MRAM layers that is similar to or the same as that used in manufacturing the magnetic read sensors in hard disk drives.

The increasing demand for nonvolatile memory based upon MRAM and STT MRAM will cause total manufacturing equipment revenue used for making the MRAM devices to rise from an estimated $30M in 2021 to between $235M to $2.9B by 2032 with a baseline projected spending of $1.5B.

METHODOLOGY

The report presents data collected through careful interviews participants on all sides of the emerging memory market: Developers, vendors, licensors and licensees, tool makers, foundries, etc. Data was collected by Coughlin Associates and Objective Analysis via field interviews and at trade conferences and seminars. Forecast data has been derived from primary and secondary sources, along with Objective Analysis' highly-regarded trend analysis of memory chip pricing and supply/demand dynamics. Extensive reading of widespread sources provided insight in technical areas. In certain cases, analyst judgment was called upon to expand upon the data that was available through these sources.

FURTHER READING

The following references are included for those who wish to gain a deeper understanding of the issues discussed in this report:

The Micron/Intel 3D XPoint Memory
Objective Analysis In-Depth Report
http://Objective-Analysis.com/reports/#XPoint

Jim Handy's memory blog: ***The Memory Guy***
http://www.TheMemoryGuy.com

Tom Coughlin's Forbes.com Blog : ***Storage Bytes***
https://www.forbes.com/sites/tomcoughlin

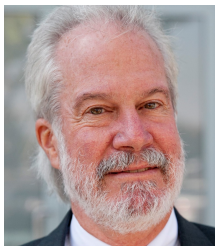
AUTHORS

Tom Coughlin

Tom Coughlin has worked for over 40 years in the data storage industry and is President of Coughlin Associates, Inc.. He has over 500 publications and six patents and is a frequent public speaker. Tom is active with the IEEE, SMPTE, SNIA, and other professional organizations. Dr. Coughlin is an IEEE Fellow and HKN member. He is co-chair of the iNEMI Mass Storage Technical Working Group, Education Chair for SNIA CSMI, Past-President of IEEE-USA and a board member of the IEEE Consultants Network of Silicon Valley. His publications include the ***Digital Storage Technology Newsletter***, ***Media and Entertainment Storage Report, and The Emerging Memory Storage Report***. Tom is the author of ***Digital Storage in Consumer Electronics: The Essential Guide***, now in its second edition with Springer. He has a regular Forbes.com blog called ***Storage Bytes*** and does a regular digital storage column for the ***IEEE Consumer Electronics Magazine***.

He was the founder and organizer of the ***Storage Visions Conferences*** as well as the ***Creative Storage Conferences***. He was general Chairman of the annual Flash Memory Summit for 10 years. Coughlin Associates provides market and technology analysis as well as data storage technical and market consulting. For more information go to www.TomCoughlin.com

Jim Handy



Jim Handy, a widely recognized semiconductor analyst, comes to Objective Analysis with over 30 years in the electronics industry including over 20 years as an industry analyst for Dataquest (now Gartner), Semico Research, and Objective Analysis. His background includes marketing and design positions at market-leading suppliers including Intel, National Semiconductor, and Infineon.

Mr. Handy is a member of the Mass Storage Technical Working Group of the International Electronics Manufacturing Initiative (iNEMI), and a member of the Storage Networking Industry Association (SNIA) Compute, Memory, and Storage Initiative (SSSI). He is also a Leader in the GLG Councils of Advisors, and serves on the Advisory Boards of the Flash Memory Summit. He is the author of three blogs covering memory chips (www.TheMemoryGuy.com), SSDs (www.TheSSDguy.com), and semiconductors for the investor (www.Smartkarma.com and formerly blogs.Forbes.com/JimHandy). He contributes from time to time to a number of other blogs.

A frequent presenter at trade shows, Mr. Handy is known for his widespread industry presence and volume of publication. He has written hundreds of articles for trade journals, Dataquest, Semico, and others, and is frequently interviewed and quoted in the electronics trade press and other media.

Mr. Handy has a strong technical leaning, with a Bachelor's degree in Electrical Engineering from Georgia Tech, and is a patent holder in the field of cache memory design. He is the author of ***The Cache Memory Book*** (Harcourt Brace, 1993), the leading reference in the field. Handy also holds an MBA degree from the University of Phoenix. He has performed rigorous technical analysis on the economics of memory manufacturing and sales, discrediting some widely held theories while unveiling other true motivators of market behavior.

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