EMERGING MEMORIES TAKE OFF

COUGHLIN ASSOCIATES
San Jose, California

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and

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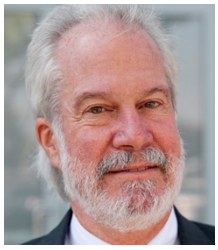
Tom Coughlin has worked for over 40 years in the data storage industry and is President of Coughlin Associates, Inc.. He has over 500 publications and six patents and is a frequent public speaker. Tom is active with the IEEE, SMPTE, SNIA, and other professional organizations. Dr. Coughlin is an IEEE Fellow and HKN member. He is co-chair of the iNEMI Mass Storage Technical Working Group, Education Chair for SNIA CSMI, Past-President of IEEE-USA and a board member of the IEEE Consultants Network of Silicon Valley. His publications include the ***Digital Storage Technology Newsletter***, ***Media and Entertainment Storage Report, and The Emerging Memory Storage Report***. Tom is the author of ***Digital Storage in Consumer Electronics: The Essential Guide***, now in its second edition with Springer. He has a regular Forbes.com blog called ***Storage Bytes*** and does a regular digital storage column for the ***IEEE Consumer Electronics Magazine***.

He was the founder and organizer of the ***Storage Visions Conferences*** as well as the ***Creative Storage Conferences***. He was general Chairman of the annual Flash Memory Summit for 10 years. Coughlin Associates provides market and technology analysis as well as data storage technical and market consulting. For more information go to www.TomCoughlin.com



Jim Handy, Principal Analyst, Objective Analysis:
Jim Handy, a widely recognized semiconductor analyst, comes to Objective Analysis with over 30 years in the electronics industry including over 20 years as an industry analyst for Dataquest (now Gartner), Semico Research, and Objective Analysis. His background includes marketing and design positions at market-leading suppliers including Intel, National Semiconductor, and Infineon.

Mr. Handy is a member of the Mass Storage Technical Working Group of the International Electronics Manufacturing Initiative (iNEMI), and a member of the Storage Networking Industry Association (SNIA) Compute, Memory, and Storage Initiative (SSSI). He is also a Leader in the GLG Councils of Advisors, and serves on the Advisory Boards of the Flash Memory Summit. He is the author of three blogs covering memory chips (www.TheMemoryGuy.com), SSDs (www.TheSSDguy.com), and semiconductors for the investor (www.Smartkarma.com and formerly blogs.Forbes.com/JimHandy). He contributes from time to time to a number of other blogs.

A frequent presenter at trade shows, Mr. Handy is known for his widespread industry presence and volume of publication. He has written hundreds of articles for trade journals, Dataquest, Semico, and others, and is frequently interviewed and quoted in the electronics trade press and other media.

Mr. Handy has a strong technical leaning, with a Bachelor's degree in Electrical Engineering from Georgia Tech, and is a patent holder in the field of cache memory design. He is the author of ***The Cache Memory Book*** (Harcourt Brace, 1993), the leading reference in the field. Handy also holds an MBA degree from the University of Phoenix. He has performed rigorous technical analysis on the economics of memory manufacturing and sales, discrediting some widely held theories while unveiling other true motivators of market behavior.

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EXECUTIVE SUMMARY

Current memory technologies including flash memory (NAND and NOR), DRAM and SRAM are facing potential technology limits to their continued improvement. As a result, there are intense efforts to develop new memory technologies. Most of these new technologies are nonvolatile memories and can be used for long-term storage or to provide a memory that retains information when powered down. This offers advantages for battery and ambient powered devices and also for energy savings in data centers.

The memories addressed in this report include PCM, ReRAM, FRAM, Toggle MRAM, STT MRAM and a variety of less mainstream technologies such as carbon nanotubes. Based upon the level of current development and the characteristics of these technologies, resistive RAM (ReRAM) may be a potential replacement for flash memory. However, NAND flash memory has several generations of technologies that will be implemented before a replacement is required. Thus, this transition will not fully occur until the next decade at the earliest.

Micron and Intel's introduction of 3D XPoint memory, a technology that has high endurance, performance much better than NAND, although somewhat slower than DRAM, and higher density than DRAM, could impact the need for DRAM. Intel introduced NVMe SSDs with its Optane technology (using 3D XPoint) in 2017 and began to ship NVDIMM Optane products in 2019, in support of its newest generation of server processors, the Second-Generation Intel Xeon Scalable Processors. 3D XPoint uses a type of phase change technology.

Magnetic RAM (MRAM) and spin transfer torque RAM (STT MRAM) will start to replace some NOR flash, SRAM and possibly DRAM within the next few years and probably before ReRAM replaces NAND flash memory. The rate of development in STT MRAM and MRAM capabilities will gradually result in lower prices, and the attractiveness of replacing volatile memory with high speed and high endurance nonvolatile memory make these technologies very competitive, assuming that their volume increases to reduce production costs (and thus purchase prices).

Ferroelectric RAM (FRAM) and some ReRAM technologies have some niche applications and with the use of HfO FRAM the number of niche markets available for FRAM could increase.

Moving to a nonvolatile solid-state main memory and cache memory will reduce power usage directly as well as enable new power saving modes, provide faster recovery from power off and enable more stable computer architectures that retain their state even when power is off. Eventually spintronic technology, that uses spin rather than current for logic functions, could be used to make future microprocessors. Spin-based logic could enable very efficient in-memory computing. Several emerging memory technologies are also being used in neuromorphic computing experiments.

The use of a nonvolatile technology as an embedded memory combined with CMOS logic has great importance in the electronics industry. NOR flash reached its scaling limit at 28nm, and soon will be replaced with one of these new technologies. As a replacement for a multi-transistor SRAM, STT MRAM could dramatically reduce the number of memory transistors and thus provide a low cost, higher-density solution.

A number of enterprise and consumer devices use MRAM, based on field switching, to act as an embedded cache memory, and this trend will continue.

The availability of STT MRAM has accelerated this trend. Because of the compatibility of MRAM and STT-RAM processes with conventional CMOS processes, these memories can be built directly on top of CMOS logic wafers. Flash memory doesn't have the same compatibility with conventional CMOS. The power savings of nonvolatile and simpler MRAM and STT MRAM when compared with SRAM is significant. As MRAM $/GB costs approach those of SRAM, this replacement could cause significant market expansion.

We project that 3D XPoint memory, with significant gigabyte shipments in 2020-2021, and with its important price advantage versus DRAM, will grow to a baseline level of 552EB (exabytes) of shipping capacity by 2031. 3D XPoint baseline revenues are projected to reach $20.6B by 2031.

It is projected that total MRAM and STT MRAM baseline annual shipping capacity will rise from an estimated 40TB in 2020 to 991PB in 2031. Total MRAM and STT-RAM baseline revenues are expected to increase from $43M in 2020 to about $24B by 2031. Much of this revenue gain will be at the expense of SRAM, NOR flash and some DRAM, although STT-RAM is developing its own special place in the pantheon of shipping memory technologies.

The demand for MRAM and STT-MRAM will drive demand for capital equipment to manufacture these devices. While MRAM and STT-MRAM can be built on standard CMOS circuits supplied by large semiconductor fabricators, MRAM and STT MRAM do require specialized fabrication equipment for the MRAM layers that is similar to or the same as that used in manufacturing the magnetic read sensors in hard disk drives.

The increasing demand for nonvolatile memory based upon MRAM and STT MRAM will cause total manufacturing equipment revenue used for making the MRAM devices to rise from an estimated $9.9M in 2020 to between $208M to $2.4B by 2031 with a baseline projected spending of $1.2B.

OBJECTIVE ANALYSIS
Semiconductor Market Research

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This report, jointly produced by Objective Analysis and Coughlin Associates, provides an exhaustive look at emerging memory technologies and their interaction with standard memories, both as discrete devices and in embedded applications (the memories within logic chips like ASICs and MCUs). The report provides a well of technical information, market dynamics, forecasts, and competitive analyses of the leading companies. Forecasts show how the markets will grow not only for the technologies themselves, but also for the capital equipment used to produce them. Read this to understand the competitive landscape and market drivers for these new memories, and to learn how to profit from tomorrow's market.

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