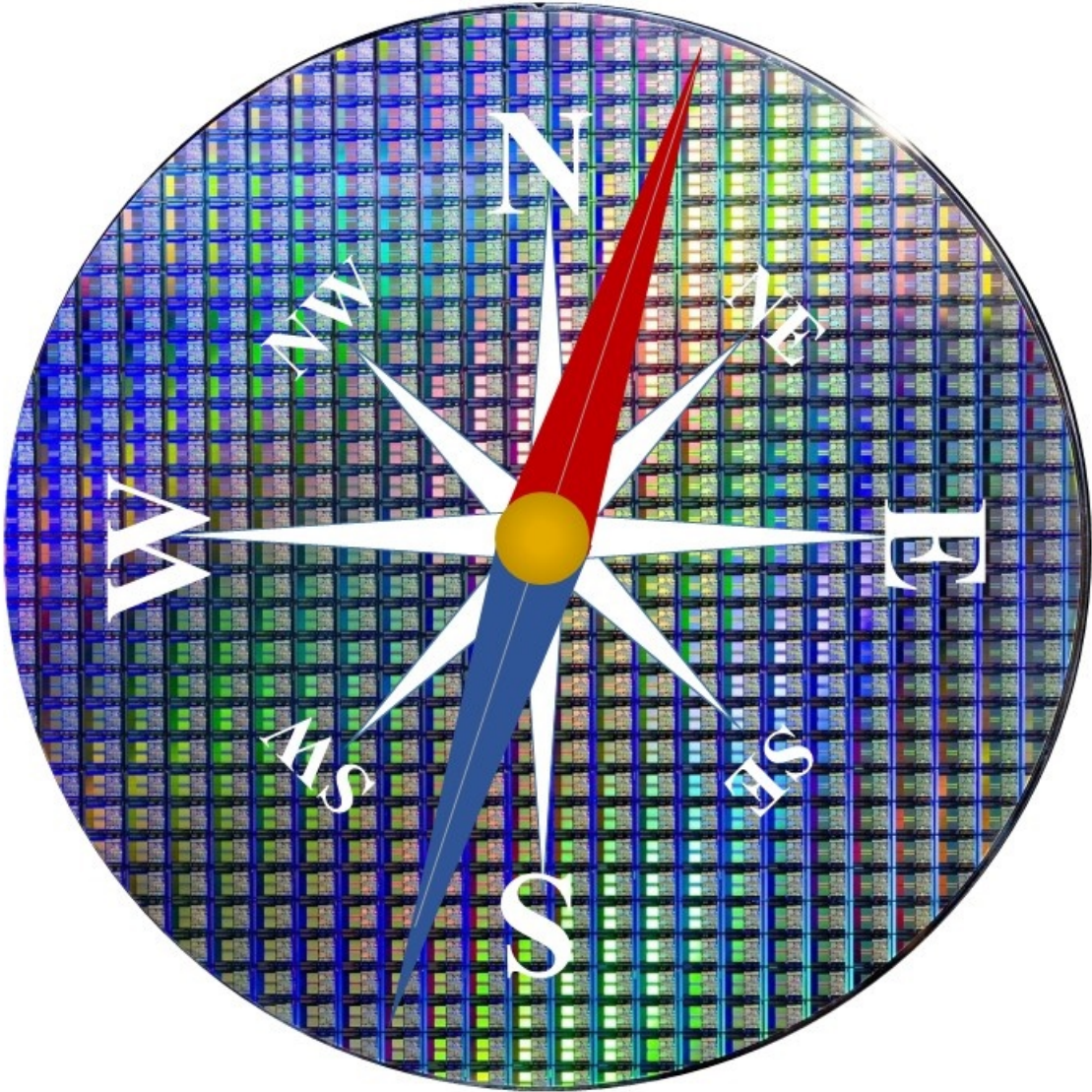


EMERGING MEMORIES FIND THEIR DIRECTION



COUGHLIN ASSOCIATES
San Jose, California
June 2020

EMERGING MEMORIES FIND THEIR DIRECTION

**Dr. Tom Coughlin, Coughlin Associates
and
Jim Handy, Objective Analysis**

**COUGHLIN ASSOCIATES
SAN JOSE, CALIFORNIA**

The ***EMERGING MEMORIES FIND THEIR DIRECTION, An Emerging Memory Report*** is published by:

Coughlin Associates
9460 Carmel Road
Atascadero, Ca. 93422

Tel (408) 202-5098
FAX (866) 374-6345
Email: info@tomcoughlin.com

© Copyright June 2020 Coughlin Associates

All rights reserved. No portion of this report may be reproduced in any form or by any means without permission from the publisher. Information in this report is believed to be reliable but cannot be guaranteed to be complete or correct

TABLE OF CONTENTS

	PAGE
.....	
THE AUTHORS.....	16
EXECUTIVE SUMMARY.....	17
INTRODUCTION.....	19
WHY EMERGING MEMORIES ARE POPULAR.....	23
SCALING LIMITS FOR ENTRENCHED TECHNOLOGIES	23
3D NAND FLASH TECHNOLOGIES	23
FUTURE FLASH MEMORIES.....	27
EMBEDDED NOR AND SRAM SCALING CHALLENGES.....	28
STANDALONE NAND & DRAM SCALING CONCERNS.....	30
TECHNICAL ADVANTAGES	31
POTENTIAL COST/GB ADVANTAGES.....	32
WHICH APPLICATIONS WANT EMERGING MEMORIES FIRST?	32
HOW A NEW MEMORY LAYER IMPROVES COMPUTER PERFORMANCE	33
HOW PERSISTENCE CHANGES THE MEMORY/STORAGE HIERARCHY (STORAGE CLASS MEMORIES)	33
STANDARDIZING THE PERSISTENT MEMORY SOFTWARE INTERFACE.....	38
IN-MEMORY COMPUTING POSSIBILITIES.....	39
UNDERSTANDING BIT SELECTORS.....	40
RESISTIVE RAM, RERAM, RRAM, MEMRISTOR:.....	48
RERAM DEVICE FUNCTION.....	49
3D RESISTIVE RAM TECHNOLOGY	55
RERAM CMOS INTEGRATION.....	55
3D NAND APPROACH TO RERAM	57
RERAM AND ARTIFICIAL INTELLIGENCE	57
CURRENT RERAM STATUS.....	59
FERROELECTRIC RAM, FERAM, FRAM.....	60
OPERATION OF FRAM	65
FRAM DEVICE CHARACTERISTICS.....	67
FERROELECTRIC FIELD EFFECT TRANSISTOR RAM (FEFET).....	69
3D FEFET FRAM.....	69
ANTIFERROELECTRICS AND FERROELECTRIC TUNNEL JUNCTIONS.....	70
THE FUTURE OF FRAM.....	71
PHASE CHANGE MEMORY (PCM):.....	72

OPERATION OF PCM.....	72
ADVANTAGES AND DISADVANTAGES.....	75
PCM APPLICATIONS.....	76
INTEL/MICRON 3D CROSSPOINT MEMORY.....	77
APPLICATIONS.....	78
MRAM (MAGNETIC RAM), STT MRAM (SPIN TRANSFER TORQUE MRAM)....	81
MRAM.....	81
STT MRAM.....	84
HOW STT WORKS.....	87
STT MANUFACTURE.....	89
STT STRENGTHS & WEAKNESSES.....	90
MERAM, AN ALTERNATIVE SPIN MEMORY DEVICE.....	97
MRAM IN ARTIFICIAL INTELLIGENCE.....	99
OTHER EMERGING MEMORY TYPES.....	101
CARBON NANOTUBES (CNTs):.....	101
POLYMERIC FERROELECTRIC RAM (PFRAM).....	103
III-V FLOATING GATE.....	104
LITHOGRAPHY:.....	104
MULTI-PATTERNING:.....	105
FUTURE LITHOGRAPHY.....	106
<i>Nano-Imprinting Lithography</i>	106
EXTREME UV (EUV) TECHNOLOGY.....	110
3D MEMORY CIRCUIT DESIGN:.....	113
3D MEMORY CIRCUIT APPROACHES.....	114
SUMMARY OF SOLID-STATE MEMORY & STORAGE TECHNOLOGIES	115
EMERGING MEMORIES AND NEW MATERIALS.....	118
EMERGING MEMORY PROCESS EQUIPMENT.....	120
MRAM AND STT MRAM PROCESS EQUIPMENT.....	122
<i>Physical Vapor Deposition</i>	125
<i>Ion Beam and Plasma Etching</i>	133
<i>Photolithography (Patterning)</i>	140
<i>Other Process Equipment</i>	142
<i>Device Testing</i>	143
<i>MRAM and STT MRAM Consortia</i>	148
PHASE CHANGE MANUFACTURING EQUIPMENT.....	149
MEMORY IS DRIVING SEMICONDUCTOR CAPITAL SPENDING.....	150
MARKET PROJECTIONS FOR MRAM, AND 3D XPOINT MEMORY.....	153
MRAM SCENARIO ESTIMATES.....	160
3D XPOINT BANDED ESTIMATES.....	166

COMBINED EMERGING MEMORY ESTIMATES	169
ESTIMATES OF MRAM CAPITAL EQUIPMENT DEMAND	173
ION BEAM ETCHING EQUIPMENT	174
PATTERNING EQUIPMENT	176
PHYSICAL VAPOR DEPOSITION EQUIPMENT.....	178
TEST AND OTHER EQUIPMENT.....	180
SUMMARY OF MRAM EQUIPMENT DEMAND	182
COMPANY INFORMATION:	185
MEMORY AND APPLICATIONS COMPANIES	185
SEMICONDUCTOR FAB COMPANIES	195
CAPITAL EQUIPMENT COMPANIES	196

LIST OF TABLES

TABLE	PAGE
TABLE 1. COMPARISON OF VARIOUS SOLID STATE MEMORY TECHNOLOGIES.....	35
TABLE 2. SUMMARY OF EMERGING MEMORY TECHNOLOGIES	117
TABLE 3. SOME MRAM PROCESS EQUIPMENT VENDORS.....	125
TABLE 4. \$/GB ESTIMATES FOR BASELINE STANDALONE DRAM, NAND, NOR, SRAM, MRAM AND 3D XPOINT FROM 2018 THROUGH 2030.....	154
TABLE 5. ANNUAL BASELINE PETABYTE SHIPMENTS FOR VARIOUS STANDALONE MEMORY TECHNOLOGIES FROM 2018 THROUGH 2030 .	156
TABLE 6. ASSUMPTIONS FOR BASELINE STANDALONE MRAM MODEL	157
TABLE 7. ANNUAL BASELINE REVENUE ESTIMATES FOR VARIOUS STANDALONE MEMORY TECHNOLOGIES FROM 2019 THROUGH 2030 (\$M)	159
TABLE 8. COMPARISON OF STANDALONE MRAM MEMORY WAFER ESTIMATES FOR THREE SCENARIOS COMPARED TO BASELINE CASE	160
TABLE 9. COMPARISON OF EMBEDDED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE	161
TABLE 10. COMPARISON OF COMBINED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE	163
TABLE 11. ANNUAL HIGH, BASELINE AND LOW COMBINED PETABYTE SHIPMENT ESTIMATES FOR MRAM.....	164
TABLE 12. ANNUAL HIGH, BASELINE AND LOW COMBINED REVENUE ESTIMATES FOR MRAM	165
TABLE 13. ANNUAL HIGH, BASELINE AND LOW PETABYTE SHIPMENT ESTIMATES FOR 3D XPOINT.....	166
TABLE 14. ANNUAL HIGH, BASELINE & LOW REVENUE 3D XPOINT ESTIMATES.....	167

TABLE 15. HIGH COMBINED PETABYTE SHIPMENT ESTIMATES FOR MRAM AND 3D XPOINT.....	169
TABLE 16. BASELINE COMBINED PETABYTE SHIPMENT ESTIMATES FOR MRAM AND 3D XPOINT.....	169
TABLE 17. LOW COMBINED PETABYTE SHIPMENT ESTIMATES FOR MRAM AND 3D XPOINT.....	170
TABLE 18. HIGH REVENUE ESTIMATES FOR MRAM AND 3D XPOINT (\$M).....	171
TABLE 19. BASELINE REVENUE ESTIMATES FOR MRAM AND 3D XPOINT (\$M).....	171
TABLE 20. LOW REVENUE ESTIMATES FOR MRAM AND 3D XPOINT (\$M).....	172
TABLE 21. BASELINE EQUIPMENT SHIPMENT ESTIMATES FOR MRAM ION BEAM ETCHING EQUIPMENT FROM 2019 THROUGH 2030.....	174
TABLE 22. ANNUAL BASELINE SPENDING ESTIMATES FOR MRAM ION BEAM ETCHING EQUIPMENT FROM 2019 THROUGH 2030 (\$M).....	175
TABLE 23. BASELINE EQUIPMENT ESTIMATES FOR MRAM PATTERNING EQUIPMENT FROM 2019 THROUGH 2030.....	176
TABLE 24. BASELINE ANNUAL REVENUE ESTIMATES FOR MRAM PATTERNING EQUIPMENT FROM 2018 THROUGH 2030 (\$M).....	177
TABLE 25. BASELINE EQUIPMENT ESTIMATES FOR MRAM PHYSICAL VAPOR DEPOSITION EQUIPMENT FROM 2019 THROUGH 2030.....	178
TABLE 26. BASELINE ANNUAL SPENDING ESTIMATES FOR MRAM PHYSICAL DEPOSITION EQUIPMENT FROM 2019 THROUGH 2030 (\$M).....	179
TABLE 27. BASELINE EQUIPMENT UNIT ESTIMATES FOR MRAM TEST AND OTHER EQUIPMENT FROM 2019 THROUGH 2030.....	180
TABLE 28. PRICE ESTIMATES FOR MRAM TEST AND OTHER EQUIPMENT FROM 2019 THROUGH 2030 (\$M).....	180
TABLE 29. BASELINE ANNUAL SPENDING ESTIMATES FOR MRAM TEST AND OTHER EQUIPMENT FROM 2019 THROUGH 2030 (\$M).....	181
TABLE 30. BASELINE EQUIPMENT UNIT SHIPMENT ESTIMATES FOR MRAM EQUIPMENT FROM 2019 THROUGH 2030.....	182
TABLE 31. ANNUAL BASELINE SPENDING ESTIMATES FOR MRAM EQUIPMENT FROM 2019 THROUGH 2030 (\$M).....	183

LIST OF FIGURES

FIGURE	PAGE
FIGURE 1. MEMORY DENSITY AND POWER REQUIREMENTS BY APPLICATION CATEGORY	19
FIGURE 2. SOLID-STATE MEMORY/STORAGE TECHNOLOGIES.....	21
FIGURE 3. 3D NAND FLASH MEMORY TOPOLOGY.....	24
FIGURE 4. TOSHIBA'S BICS AND SAMSUNG'S TCAT 3D NAND STRUCTURES	25
FIGURE 5. COST OF TRANSITION FROM ONE NAND MANUFACTURING PROCESS TO THE NEXT	26
FIGURE 6. PROJECTED NAND FLASH CHIP TECHNOLOGY ROADMAP... 	28
FIGURE 7. SRAM CELL SIZES SHRINK MORE SLOWLY THAN PROCESSES	29
FIGURE 8. COMPARISON OF MEMORY AND STORAGE TECHNOLOGIES BY PRICE PER GIGABYTE AND PERFORMANCE.....	34
FIGURE 9. EVERS PIN 1 GB STT MRAM CHIP	36
FIGURE 10. PROGRESSION OF STORAGE TECHNOLOGIES WITH NONVOLATILE SOLID-STATE STORAGE	37
FIGURE 11. CONTRIBUTORS TO NONVOLATILE SOLID-STATE STORAGE LATENCY WITH LEGACY AND CURRENT SOLID-STATE NONVOLATILE TECHNOLOGIES.....	39
FIGURE 12. RERAM SYSTEM ON CHIP	39
FIGURE 13. BIT SELECTORS - 3-TERMINAL (LEFT) 2-TERMINAL (RIGHT)	41
FIGURE 14. OVERHEAD VIEW OF A SIMPLE CROSSPOINT ARRAY	41
FIGURE 15. READING WHEN ONE BIT IS IN A LOW-RESISTANCE STATE	42
FIGURE 16. SNEAK PATHS OCCUR WHEN MULTIPLE BITS ARE IN A LOW RESISTANCE STATE.....	43
FIGURE 17. SPACE PENALTY OF A 3-TERMINAL SELECTOR	44

FIGURE 18. BIDIRECTIONAL DIODE SELECTOR	45
FIGURE 19. A 1TNR SELECTOR CONFIGURATION	46
FIGURE 20. 3D CROSSPOINT ARRAY STACKING	47
FIGURE 21. STACKED CROSSPOINT MEMORY ARRAY	47
FIGURE 22. RERAM FILAMENT CELL CONDUCTION AND SWITCHING	49
FIGURE 23. RERAM SCALING.....	50
FIGURE 24. RERAM RESISTANCE SCALING.....	50
FIGURE 25. TAOX RERAM DEVICE.....	52
FIGURE 26. CURRENT LEVELS AND VOLTAGES FOR RERAM SWITCHING.....	52
FIGURE 27. COMPARING CERAM CELL STRUCTURE TO RERAM	53
FIGURE 28. RERAM STACKED CROSSPOINT ARRAY	54
FIGURE 29. RERAM MEMORY BANK	55
FIGURE 30. RERAM CMOS INTEGRATION.....	56
FIGURE 31. TWO-MASK RERAM ELEMENT IN TUNGSTEN VIAS	56
FIGURE 32. 3D RERAM STRUCTURE/PROCESS.....	57
FIGURE 33. A SIMPLIFIED VIEW OF A NEURAL NETWORK.	58
FIGURE 34. EARLY FERROELECTRIC MEMORY - 1955 BELL LABS 256-BIT DEVICE	61
FIGURE 35. HYSTERESIS CURVE OF FERROELECTRIC MEMORY	62
FIGURE 36. PUBLICATION COUNT FOR FEFET RESEARCH PAPERS	63
FIGURE 37. AMORPHOUS, CRYSTALLINE, AND FERROELECTRIC HAFNIUM OXIDE	64
FIGURE 38. PZT AND HFO CAPACITORS, SHOWING TYPICAL DIMENSIONS.....	65
FIGURE 39. FRAM PEROVSKITE DISPLACEMENT	66
FIGURE 40. MEMORY PROPERTIES OF FERROELECTRIC HAFNIUM OXIDE AS DERIVED FROM EXPERIMENTS AND EXPECTED MATERIAL LIMITS	67

FIGURE 41. FRAM PLANAR CELL STRUCTURE	68
FIGURE 42. FEFET TRANSISTOR	69
FIGURE 43. 3D HAFNIUM OXIDE FRAM BUILT USING 3D NAND TECHNIQUES	70
FIGURE 44. CROSSPOINT MEMORY USING PCM CELLS	72
FIGURE 45. CHARACTERISTICS OF THE READ, WRITE AND ERASE CYCLE FOR PCM MATERIALS	73
FIGURE 46. PCM MEMORY CELL.....	74
FIGURE 47. CROSS SECTION OF PCM CELL	74
FIGURE 48. STMICROELECTRONICS' TRANSISTOR-SELECTED PCM CELL	75
FIGURE 49. INTEL'S VIEW OF THE MEMORY-STORAGE HIERARCHY	79
FIGURE 50. REDIS VIRTUAL MACHINE COUNT VS. MEMORY SIZE	80
FIGURE 51. BASIC CELL DIAGRAM FOR FIELD SWITCHED MRAM	81
FIGURE 52. FIELD SWITCHED ARRAY MRAM ARCHITECTURE.....	82
FIGURE 53. GLOBALFOUNDRIES ROADMAP FOR EMBEDDED MRAM	85
FIGURE 54. PARALLEL TO ANTIPARALLEL SWITCHING	88
FIGURE 55. SPIN TRANSFER TORQUE OPERATION.....	88
FIGURE 56. IN PLANE (A) AND PERPENDICULAR (B) MAGNETIC TUNNEL CELLS.....	89
FIGURE 57. STT MRAM CELL STRUCTURE.....	89
FIGURE 58. EVERSPIN STT MRAM DEVICE.....	90
FIGURE 59. STT MRAM CURRENT OPERATION	91
FIGURE 60. MULTI-BIT MRAM CELL READ OUT	92
FIGURE 61. A COMPARISON OF DRAM, NAND FLASH AND STT MRAM ..	93
FIGURE 62. STT MRAM CROSS SECTION	94
FIGURE 63. COMPARISON OF IDEAL MRAM, STAND-ALONE DRAM, PLANAR FLASH AND HDD MEMORY BIT DIMENSIONS.....	94

FIGURE 64. STT MRAM EMBEDDED MEMORY.....	95
FIGURE 65. COMPARISON OF STT-MRAM TO SOT-MRAM.....	97
FIGURE 66. EXAMPLE MERAM DEVICE STRUCTURE.....	98
FIGURE 67. MERAM STACK.....	98
FIGURE 68. GYRFALCON AI ACCELERATOR WITH MRAM.....	100
FIGURE 69. CNT FABRIC.....	102
FIGURE 70. PFRAM 3-LAYER POLYMERIC MEMORY.....	103
FIGURE 71. ORIGINAL SINGLE-PATTERNED FEATURES.....	105
FIGURE 72. CLAD THE SIDES OF THE ORIGINAL PATTERN.....	105
FIGURE 73. REMOVE THE ORIGINAL PATTERN. THE REMAINING CLADDING IS A DOUBLED PATTERN.....	106
FIGURE 74. CLAD THE SIDES OF THE DOUBLED PATTERN.....	106
FIGURE 75. REMOVE THE DOUBLED PATTERN. THE REMAINING CLADDING IS THE QUADRUPLED PATTERN.....	106
FIGURE 76. NANOIMPRINT PROCESS.....	108
FIGURE 77. NANOIMPRINT DEPRESSIONS.....	109
FIGURE 78. FLUID DISPENSE PROCESS.....	109
FIGURE 79. LIGHT SPECTRUM.....	110
FIGURE 80. EUV SCANNING LITHOGRAPHIC EXPOSURE SYSTEM.....	111
FIGURE 81. BIT DENSITY OF LARGEST MEMORIES PRESENTED AT IEEE RESEARCH CONFERENCES, 2001-2019.....	116
FIGURE 82. FUTURE MEMORY/STORAGE HIERARCHY.....	118
FIGURE 83. EXAMPLE ELEMENTS TO ENABLE NEW MEMORIES.....	119
FIGURE 84. COMPARISON OF MULTIPLE EMERGING MEMORY CELL STRUCTURES.....	120
FIGURE 85. MRAM MEMORY CELL.....	122

FIGURE 86. CROSS-SECTION OF AN MRAM DEVICE SHOWING DETAILS OF THE CMOS SUBSTRATE AND MAGNETIC LAYERS FABRICATED ON TOP OF THE SUBSTRATE	123
FIGURE 87. MRAM MANUFACTURING PROCESS FLOW	124
FIGURE 88. KEY MRAM PROCESS EQUIPMENT.....	124
FIGURE 89. APPLIED MATERIALS CMP SYSTEM.....	126
FIGURE 90. APPLIED MATERIALS ENDURA PLATFORM	127
FIGURE 91. CANON ANELVA EC7800 PVD EQUIPMENT.....	128
FIGURE 92. CANON ANELVA NC7900 PVD EQUIPMENT	128
FIGURE 93. SINGULUS TIMARIS II PVD CLUSTER TOOL PLATFORM.....	129
FIGURE 94. SINGULUS PVD CLUSTER TOOL PLATFORMS	129
FIGURE 95. TOKYO ELECTRON EXIM PVD CLUSTER TOOL PLATFORM	131
FIGURE 96. ULVAC MAGEST S200 MULTILAYER THIN FILM DEPOSITION SYSTEM.....	132
FIGURE 97. VEECO NEXUS IBD ION BEAM DEPOSITION SYSTEM	132
FIGURE 98. A THREE GRID ION BEAM EXTRACTION SYSTEM.....	133
FIGURE 99. SCHEMATIC OF MTJ ETCHING PROCESS	134
FIGURE 100. APPLIED MATERIALS CENTURA TOOL	134
FIGURE 101. APPLIED MATERIALS PRODUCER SYSTEM.....	135
FIGURE 102. CANON ANELVA NC8000 ION BEAM ETCH MACHINE.....	135
FIGURE 103. HITACHI HIGH TECHNOLOGY E-600/8000 NONVOLATILE ETCH SYSTEM.....	136
FIGURE 104. LAM RESEARCH KIYO ION BEAM ETCHING CHAMBER	137
FIGURE 105. OXFORD INSTRUMENTS IONFAB 300 IBE SYSTEM.....	138
FIGURE 106. PLASMA THERM PINNACLE ION BEAM ETCH AND DEPOSITION SYSTEM.....	138
FIGURE 107. ULVAC ULHITE NE-7800H NON-VOLATILE MATERIAL ETCHING TOOL	139

FIGURE 108. VEECO NEXUS IBE-420I ION BEAM ETCHING SYSTEM	140
FIGURE 109. ASML DEEP UV PHOTOLITHOGRAPHY TOOL	141
FIGURE 110. NIKON PHOTOLITHOGRAPHIC PRODUCT LINES	141
FIGURE 111. CANON LITHOGRAPHIC I-LINE STEPPER PRODUCT LINE	142
FIGURE 112. TOKYO ELECTRON MRT300 MAGNETIC ANNEALING TOOL	143
FIGURE 113. ISI WLA 3000 WAFER LEVEL QUASI-STATIC TESTER	144
FIGURE 114. HPROBE 3D HIGH MAGNETIC FIELD WAFER PROBE	145
FIGURE 115. KEYSIGHT TECHNOLOGY NX5730A MRAM TEST PLATFORM	145
FIGURE 116. MICROSENSE (KLA/TENCOR) POLAR KERR SYSTEM FOR PERPENDICULAR STT MRAM.....	146
FIGURE 117. AFM EQUIPMENT	147
FIGURE 118. APPLIED MATERIALS ENDURA IMPULSE FOR PCM AND RERAM	149
FIGURE 119. SEMI'S WAFER FAB EQUIPMENT SPENDING HISTORY AND FORECAST.....	150
FIGURE 120. EQUIPMENT SPENDING BY REGION	151
FIGURE 121. NUMBER OF VOLUME FABs STARTING BY REGION (ALL SEMICONDUCTORS, INCLUDING DISCRETES).....	152
FIGURE 122. PROFITABILITY OF NAND FLASH MANUFACTURERS	153
FIGURE 123. CHART OF BASELINE \$/GB FOR STANDALONE MEMORY TECHNOLOGIES FROM 2018 THROUGH 2020	155
FIGURE 124. CHART OF ANNUAL BASELINE PETABYTE SHIPMENTS FOR STANDALONE MEMORY TECHNOLOGIES FROM 2018 THROUGH 2030 .	157
FIGURE 125. CHART OF BASELINE REVENUE ESTIMATES FOR MEMORY TECHNOLOGIES FROM 2019 THROUGH 2030 (\$M).....	159
FIGURE 126. CHART OF STANDALONE MRAM MEMORY WAFER ESTIMATES FOR THREE SCENARIOS COMPARED TO BASELINE CASE.....	161
FIGURE 127. CHART OF EMBEDDED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE	162

FIGURE 128. CHART OF COMBINED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE 163

FIGURE 129. CHART OF COMBINED MRAM MEMORY PETABYTE SHIPMENT ESTIMATES FOR HIGH/LOW SCENARIOS COMPARED TO BASELINE CASE 164

FIGURE 130. CHART OF COMBINED MRAM MEMORY REVENUE ESTIMATES FOR HIGH/LOW SCENARIOS COMPARED TO BASELINE CASE..... 165

FIGURE 131. CHART OF HIGH, BASELINE AND LOW PETABYTE SHIPPING ESTIMATES FOR 3D XPOINT..... 167

FIGURE 132. CHART OF HIGH, BASELINE AND LOW REVENUE 3D XPOINT ESTIMATES..... 168

FIGURE 133. CHART OF COMBINED HIGH, BASELINE AND LOW PETABYTE SHIPPING ESTIMATES FOR EMERGING MEMORIES 170

FIGURE 134. CHART OF HIGH, BASELINE AND LOW REVENUE ESTIMATES FOR EMERGING MEMORIES (\$M)..... 172

FIGURE 135. CAPITAL EQUIPMENT ESTIMATE PROCESS FLOW 173

FIGURE 136. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM ION BEAM ETCH EQUIPMENT FROM 2019 THROUGH 2030 . 175

FIGURE 137. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM PATTERNING EQUIPMENT FROM 2019 THROUGH 2030 (\$M)177

FIGURE 138. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM PHYSICAL VAPOR EQUIPMENT FROM 2019 THROUGH 2030 (\$M) 179

FIGURE 139. CHART OF BASELINE SPENDING ESTIMATES FOR MRAM TEST AND OTHER EQUIPMENT FROM 2019 THROUGH 2030 (\$M) 181

FIGURE 140. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM TEST AND OTHER EQUIPMENT FROM 2019 THROUGH 2030 (\$M) 182

FIGURE 141. CHART OF BASELINE SPENDING ESTIMATES FOR MRAM EQUIPMENT FROM 2019 THROUGH 2030 (\$M) 183

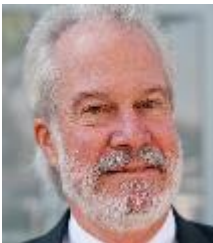
FIGURE 142. CHART OF LOW, BASELINE AND HIGH TOTAL SPENDING ESTIMATES FOR MRAM EQUIPMENT FROM 2019 TO 2030 (\$M) 184

THE AUTHORS



Tom Coughlin, President, Coughlin Associates: Tom Coughlin has worked for over 39 years in the data storage industry. He has over 1,000 publications and six patents. Tom is active with the IEEE, SMPTE, SNIA, and other professional organizations. Dr. Coughlin is an IEEE Fellow. He is co-chair of the iNEMI Mass Storage Technical Working Group, Education Chair for SNIA SSSI, Past-President of IEEE-USA and a member of the IEEE Consultants Network of Silicon Valley. His publications include the Digital Storage Technology Newsletter, Media and Entertainment Storage Report and other reports. Tom is the author of Digital Storage in Consumer Electronics: The Essential Guide, now in its second edition with Springer. He has a regular Forbes.com blog called Storage Bytes and does a regular digital storage column for the IEEE Consumer Electronics Magazine.

He was the founder and organizer of the Storage Visions Conferences as well as the Creative Storage Conferences. He was general Chairman of the annual Flash Memory Summit for 10 years. Coughlin Associates provides market and technology analysis as well as data storage technical and market consulting. For more information go to www.tomcoughlin.com



Jim Handy, Objective Analysis:

Jim Handy, a widely recognized semiconductor analyst, comes to Objective Analysis with over 30 years in the electronics industry including over 20 years as an industry analyst for Dataquest (now Gartner), Semico Research, and Objective Analysis. His background includes marketing and design positions at market-leading suppliers including Intel, National Semiconductor, and Infineon.

Mr. Handy is a member of the Mass Storage Technical Working Group of the International Electronics Manufacturing Initiative (iNEMI), and a member of the Storage Networking Industry Association (SNIA) Solid State Storage Initiative (SSSI). He is also a Leader in the Gerson Lehrman Group Councils of Advisors, serves on the Advisory Boards of the Flash Memory Summit. He is the author of three blogs covering SSDs (www.TheSSDguy.com), memory chips (www.TheMemoryGuy.com), and semiconductors for the investor at www.Smartkarma.com, and contributes to a number of other blogs.

A frequent presenter at trade shows, Mr. Handy is known for his widespread industry presence and volume of publication. He has written hundreds of articles for trade journals, Dataquest, Semico, and others, and is frequently interviewed and quoted in the electronics trade press and other media.

EXECUTIVE SUMMARY

Current memory technologies including flash memory (NAND and NOR), DRAM and SRAM are facing potential technology limits to their continued improvement. As a result, there are intense efforts to develop new memory technologies. Most of these new technologies are nonvolatile memories and can be used for long-term storage or to provide a memory that does not lose information when power is not applied. This offers advantages for battery and ambient powered devices and also for energy savings in data centers.

The memories addressed in this report include PCM, ReRAM, FRAM, MRAM, STT MRAM and a variety of less mainstream technologies such as carbon nanotubes. Based upon the level of current development and the characteristics of these technologies, resistive RAM (ReRAM) may be a potential replacement for flash memory. However, flash memory has several generations of technologies that will be implemented before a replacement is required. Thus, this transition will not fully occur until the next decade at the earliest.

Micron and Intel's introduction of 3D XPoint Memory, a technology that has high endurance, performance much better than NAND, although somewhat slower than DRAM, and higher density than DRAM, could impact the need for DRAM. Intel introduced NVMe SSDs with its Optane technology (using 3D XPoint) in 2017 and began to ship NVDIMM Optane products in 2019, in support of its newest generation of server processors, the Second-Generation Intel Xeon Scalable Processors. 3D XPoint uses a type of phase change technology.

Magnetic RAM (MRAM) and spin transfer torque RAM (STT MRAM) will start to replace some NOR, SRAM and possibly DRAM within the next few years and probably before ReRAM replaces flash memory. The rate of development in STT MRAM and MRAM capabilities will gradually result in lower prices, and the attractiveness of replacing volatile memory with high speed and high endurance nonvolatile memory make these technologies very competitive, assuming that their volume increases to reduce production costs (and thus purchase prices).

Ferroelectric RAM (FRAM) and some ReRAM technologies have some niche applications and with the use of HfO FRAM the number of niche markets available for FRAM could increase.

Moving to a nonvolatile solid-state main memory and cache memory will reduce power usage directly as well as enable new power saving modes, provide faster recovery from power off and enable more stable computer architectures that retain their state even when power is off. Eventually spintronic technology, that uses spin rather than current for logic processes, could be used to make future microprocessors. Spin-based logic could enable very efficient in-memory processing. Several emerging memory technologies are also being used in neuromorphic computing experiments.

The use of a nonvolatile technology as an embedded memory combined with CMOS logic has great importance in the electronics industry. NOR flash reached its scaling limit at 28nm, and soon will be replaced with one of these new technologies. As a replacement for a multi-transistor SRAM, STT MRAM could reduce the number of transistors and thus provide a low cost, higher-density solution. A number of enterprise and consumer devices use MRAM, based on field switching, to act as an embedded cache memory, and this trend will continue.

The availability of STT MRAM has accelerated this trend. Because of the compatibility of MRAM and STT-RAM processes with conventional CMOS processes, these memories can be built directly on top of CMOS logic wafers. Flash memory doesn't have the same compatibility with conventional CMOS. The power savings of nonvolatile and simpler MRAM and STT MRAM when compared with SRAM is significant. As MRAM \$/GB costs approach those of SRAM, this replacement could cause significant market expansion.

We project that 3D XPoint Memory, with significant gigabyte shipments in 2020-2021, and with its important price advantage versus DRAM will grow to a baseline level of 90.0EB (exabytes) of shipping capacity by 2030. 3D XPoint baseline revenues are projected to reach \$25.3B by 2030.

It is projected that total MRAM and STT MRAM baseline annual shipping capacity will rise from an estimated 18TB in 2019 to 315PB in 2030. Standalone MRAM and STT-RAM baseline revenues are expected to increase from \$35M in 2019 to about \$10B by 2030. Much of this revenue gain will be at the expense of SRAM, NOR flash and some DRAM, although STT-RAM is developing its own special place in the pantheon of shipping memory technologies.

The demand for MRAM and STT-MRAM will drive demand for capital equipment to manufacture these devices. While MRAM and STT-MRAM can be built on standard CMOS circuits supplied by large semiconductor fabricators, MRAM and STT MRAM do require specialized fabrication equipment for the MRAM layers that is similar to or the same as that used in manufacturing the magnetic read sensors in hard disk drives.

The increasing demand for nonvolatile memory based upon MRAM and STT MRAM will cause total manufacturing equipment revenue used for making the MRAM devices to rise from an estimated \$43.8M in 2019 to between \$225M to \$1.29B by 2030 with a baseline projected spending of \$696M.

Thus, total emerging standalone memory shipments by 2030 could range from about 163.5 Exabytes to 17.2 Exabytes with a baseline value of 90.3 Exabytes. The majority of the capacity shipments are for 3D XPoint. The revenue will range between a low of about \$7.6B and a high of about \$64.7B in 2030 with a baseline value of about \$35.6B.



OBJECTIVE ANALYSIS

Semiconductor Market Research

Coughlin Associates

Data Storage Consulting

EMERGING MEMORIES FIND THEIR DIRECTION *Available June, 2020*

This report, jointly produced by Objective Analysis and Coughlin Associates, provides an exhaustive look at emerging memory technologies and their interaction with standard memories, both as discrete devices and in embedded applications (the memories within logic chips like ASICs and MCUs). The report provides a well of technical information, market dynamics, forecasts, and competitive analyses of the leading companies. Forecasts show how the markets will grow not only for the technologies themselves, but also for the capital equipment used to produce them. Read this to understand the competitive landscape and market drivers for these new memories, and to learn how to profit from tomorrow's market.

Table of Contents (Top Level):

- EXECUTIVE SUMMARY 17
- INTRODUCTION:..... 19
- WHY EMERGING MEMORIES ARE POPULAR..... 23
- HOW A NEW MEMORY LAYER IMPROVES COMPUTER PERFORMANCE 33
- UNDERSTANDING BIT SELECTORS 40
- RESISTIVE RAM, RERAM, RRAM, MEMRISTOR:..... 48
- FERROELECTRIC RAM, FERAM, FRAM:..... 60
- PHASE CHANGE MEMORY (PCM):..... 72
- INTEL/MICRON 3D CROSSPOINT MEMORY..... 77
- MRAM (MAGNETIC RAM), STT MRAM (SPIN TRANSFER TORQUE MRAM)..... 81
- OTHER EMERGING MEMORY TYPES..... 101
- LITHOGRAPHY:..... 104
- 3D MEMORY CIRCUIT DESIGN:..... 113
- SUMMARY OF SOLID-STATE MEMORY & STORAGE TECHNOLOGIES 115
- EMERGING MEMORIES AND NEW MATERIALS 118
- EMERGING MEMORY PROCESS EQUIPMENT 120
- MEMORY IS DRIVING SEMICONDUCTOR CAPITAL SPENDING..... 150
- MARKET PROJECTIONS FOR MRAM, AND 3D XPOINT MEMORY 153
- ESTIMATES OF MRAM CAPITAL EQUIPMENT DEMAND..... 173
- COMPANY INFORMATION: 185

Order at: <https://tomcoughlin.com/tech-papers/>
or <https://Objective-Analysis.com/reports/#Emerging>