EMERGING MEMORIES
RAMP UP

COUGHLIN ASSOCIATES
San Jose, California
June 2019

© 2019 Coughlin Associates and Objective Analysis
EMERGING MEMORIES RAMP UP

Dr. Tom Coughlin, Coughlin Associates
and
Jim Handy, Objective Analysis

COUGHLIN ASSOCIATES
SAN JOSE, CALIFORNIA

© 2019 Coughlin Associates and Objective Analysis
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>THE AUTHORS</td>
<td>16</td>
</tr>
<tr>
<td>EXECUTIVE SUMMARY</td>
<td>17</td>
</tr>
<tr>
<td>INTRODUCTION:</td>
<td>19</td>
</tr>
<tr>
<td>WHY EMERGING MEMORIES ARE POPULAR</td>
<td>23</td>
</tr>
<tr>
<td>Scaling Limits for Entrenched Technologies</td>
<td>23</td>
</tr>
<tr>
<td>3D NAND Flash Technologies</td>
<td>23</td>
</tr>
<tr>
<td>Future Flash Memories</td>
<td>27</td>
</tr>
<tr>
<td>Embedded NOR and SRAM Scaling Challenges</td>
<td>28</td>
</tr>
<tr>
<td>Stand-alone NAND &amp; DRAM Scaling Concerns</td>
<td>28</td>
</tr>
<tr>
<td>Technical Advantages</td>
<td>30</td>
</tr>
<tr>
<td>Potential Cost/GB Advantages</td>
<td>30</td>
</tr>
<tr>
<td>HOW A NEW MEMORY LAYER IMPROVES COMPUTER PERFORMANCE</td>
<td>31</td>
</tr>
<tr>
<td>How Persistence Changes the Memory/Storage Hierarchy (Storage Class Memories)</td>
<td>31</td>
</tr>
<tr>
<td>Standardizing the Persistent Memory Software Interface</td>
<td>36</td>
</tr>
<tr>
<td>In-Memory Computing Possibilities</td>
<td>37</td>
</tr>
<tr>
<td>UNDERSTANDING BIT SELECTORS</td>
<td>38</td>
</tr>
<tr>
<td>RESISTIVE RAM, RERAM, RRAM, Memristor:</td>
<td>46</td>
</tr>
<tr>
<td>ReRAM Device Function</td>
<td>47</td>
</tr>
<tr>
<td>3D Resistive RAM Technology</td>
<td>51</td>
</tr>
<tr>
<td>ReRAM CMOS Integration</td>
<td>52</td>
</tr>
<tr>
<td>3D NAND Approach to ReRAM</td>
<td>52</td>
</tr>
<tr>
<td>Current ReRAM Status</td>
<td>53</td>
</tr>
<tr>
<td>FERROELECTRIC RAM, FERAM, FRAM:</td>
<td>53</td>
</tr>
<tr>
<td>Operation of FeRAM</td>
<td>54</td>
</tr>
<tr>
<td>FeRAM Device Characteristics</td>
<td>55</td>
</tr>
<tr>
<td>The Future of FeRAM</td>
<td>58</td>
</tr>
<tr>
<td>PHASE CHANGE MEMORY (PCM):</td>
<td>58</td>
</tr>
<tr>
<td>Operation of PCM</td>
<td>58</td>
</tr>
<tr>
<td>Advantages and Disadvantages</td>
<td>61</td>
</tr>
<tr>
<td>PCM Applications</td>
<td>62</td>
</tr>
<tr>
<td>INTEL/MICRON 3D CROSSPOINT MEMORY</td>
<td>62</td>
</tr>
<tr>
<td>Applications</td>
<td>63</td>
</tr>
</tbody>
</table>

© 2019 Coughlin Associates and Objective Analysis
# LIST OF TABLES

<table>
<thead>
<tr>
<th>TABLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TABLE 1. COMPARISON OF VARIOUS SOLID STATE MEMORY TECHNOLOGIES</td>
<td>33</td>
</tr>
<tr>
<td>TABLE 2. SUMMARY OF EMERGING MEMORY TECHNOLOGIES</td>
<td>97</td>
</tr>
<tr>
<td>TABLE 3. SOME MRAM PROCESS EQUIPMENT VENDORS</td>
<td>102</td>
</tr>
<tr>
<td>TABLE 4. $/GB ESTIMATES FOR BASELINE STANDALONE DRAM, NAND, NOR, SRAM, MRAM AND 3D XPOINT FROM 2017 THROUGH 2029</td>
<td>130</td>
</tr>
<tr>
<td>TABLE 5. ANNUAL BASELINE PETABYTE SHIPMENTS FOR VARIOUS STANDALONE MEMORY TECHNOLOGIES FROM 2017 THROUGH 2029</td>
<td>131</td>
</tr>
<tr>
<td>TABLE 6. ASSUMPTIONS FOR BASELINE STANDALONE MRAM MODEL</td>
<td>133</td>
</tr>
<tr>
<td>TABLE 7. ANNUAL BASELINE REVENUE ESTIMATES FOR VARIOUS STANDALONE MEMORY TECHNOLOGIES FROM 2018 THROUGH 2029 ($M)</td>
<td>134</td>
</tr>
<tr>
<td>TABLE 8. COMPARISON OF STANDALONE MRAM MEMORY WAFER ESTIMATES FOR THREE SCENARIOS COMPARED TO BASELINE CASE</td>
<td>135</td>
</tr>
<tr>
<td>TABLE 9. COMPARISON OF EMBEDDED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE</td>
<td>136</td>
</tr>
<tr>
<td>TABLE 10. COMPARISON OF COMBINED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE</td>
<td>137</td>
</tr>
<tr>
<td>TABLE 11. ANNUAL HIGH, BASELINE AND LOW COMBINED PETABYTE SHIPMENT ESTIMATES FOR MRAM</td>
<td>138</td>
</tr>
<tr>
<td>TABLE 12. ANNUAL HIGH, BASELINE AND LOW PETABYTE SHIPMENT ESTIMATES FOR 3D XPOINT</td>
<td>139</td>
</tr>
<tr>
<td>TABLE 13. ANNUAL HIGH, BASELINE AND LOW REVENUE ESTIMATES FOR 3D XPOINT ($M)</td>
<td>141</td>
</tr>
<tr>
<td>TABLE 14. HIGH COMBINED PETABYTE SHIPMENT ESTIMATES FOR MRAM AND 3D XPOINT</td>
<td>142</td>
</tr>
</tbody>
</table>
## LIST OF FIGURES

<table>
<thead>
<tr>
<th>FIGURE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIGURE 1. MEMORY DENSITY AND POWER REQUIREMENTS BY APPLICATION CATEGORY</td>
<td>19</td>
</tr>
<tr>
<td>FIGURE 2. SOLID-STATE MEMORY/STORAGE TECHNOLOGIES</td>
<td>20</td>
</tr>
<tr>
<td>FIGURE 3. 3D NAND FLASH MEMORY TOPOLOGY</td>
<td>24</td>
</tr>
<tr>
<td>FIGURE 4. TOSHIBA’S BICS AND SAMSUNG’S TCAT 3D NAND STRUCTURES</td>
<td>25</td>
</tr>
<tr>
<td>FIGURE 5. COST OF TRANSITION FROM ONE NAND MANUFACTURING PROCESS TO THE NEXT</td>
<td>26</td>
</tr>
<tr>
<td>FIGURE 6. PROJECTED NAND FLASH CHIP TECHNOLOGY ROADMAP</td>
<td>28</td>
</tr>
<tr>
<td>FIGURE 7. FLASH SCALING AND ENDURANCE</td>
<td>29</td>
</tr>
<tr>
<td>FIGURE 8. COMPARISON OF MEMORY AND STORAGE TECHNOLOGIES BY PRICE PER GIGABYTE AND PERFORMANCE</td>
<td>32</td>
</tr>
<tr>
<td>FIGURE 9. EVERSIPN 1 GB STT MRAM CHIP</td>
<td>34</td>
</tr>
<tr>
<td>FIGURE 10. PROGRESSION OF STORAGE TECHNOLOGIES WITH NONVOLATILE SOLID-STATE STORAGE</td>
<td>35</td>
</tr>
<tr>
<td>FIGURE 11. CONTRIBUTORS TO NONVOLATILE SOLID-STATE STORAGE LATENCY WITH LEGACY AND CURRENT SOLID-STATE NONVOLATILE TECHNOLOGIES</td>
<td>36</td>
</tr>
<tr>
<td>FIGURE 12. RERAM SYSTEM ON CHIP</td>
<td>37</td>
</tr>
<tr>
<td>FIGURE 13. RERAM MEMORY BANK</td>
<td>38</td>
</tr>
<tr>
<td>FIGURE 14. BIT SELECTORS - 3-TERMINAL (LEFT) 2-TERMINAL (RIGHT)</td>
<td>39</td>
</tr>
<tr>
<td>FIGURE 15. OVERHEAD VIEW OF A SIMPLE CROSSPOINT ARRAY</td>
<td>39</td>
</tr>
<tr>
<td>FIGURE 16. READING WHEN ONE BIT IS IN A LOW-RESISTANCE STATE</td>
<td>40</td>
</tr>
<tr>
<td>FIGURE 17. SNEAK PATHS OCCUR WHEN MULTIPLE BITS ARE IN A LOW RESISTANCE STATE</td>
<td>41</td>
</tr>
</tbody>
</table>
FIGURE 18. SPACE PENALTY OF A 3-TERMINAL SELECTOR ........................................ 42
FIGURE 19. BIDIRECTIONAL DIODE SELECTOR ................................................... 43
FIGURE 20. A 1TNR SELECTOR CONFIGURATION .................................................. 44
FIGURE 21. 3D CROSSPOINT ARRAY STACKING ..................................................... 45
FIGURE 22. STACKED CROSSPOINT MEMORY ARRAY ......................................... 45
FIGURE 23. RERAM FILAMENT CELL CONDUCTION AND SWITCHING .... 47
FIGURE 24. RERAM SCALING ................................................................................ 48
FIGURE 25. RERAM RESISTANCE SCALING ......................................................... 48
FIGURE 26. TAOX RERAM DEVICE ................................................................... 49
FIGURE 27. CURRENT LEVELS AND VOLTAGES FOR RERAM SWITCHING .... 50
FIGURE 28. RERAM STACKED CROSSPOINT ARRAY ......................................... 50
FIGURE 29. RERAM CMOS INTEGRATION ............................................................. 52
FIGURE 30. 3D RERAM STRUCTURE/PROCESS .................................................. 52
FIGURE 31. FRAM PEROVSKITE DISPLACEMENT ............................................... 54
FIGURE 32. MEMORY PROPERTIES OF FERROELECTRIC HAFNIUM OXIDE AS
DERIVED FROM EXPERIMENTS AND EXPECTED MATERIAL LIMITS .......... 55
FIGURE 33. FRAM PLANAR CELL STRUCTURE ...................................................... 56
FIGURE 34. 3D HAFNIUM OXIDE FRAM BUILT USING 3D NAND TECHNIQUES
.......................................................................................................................... 57
FIGURE 35. CROSSPOINT MEMORY USING PCM CELLS .................................. 59
FIGURE 36. CHARACTERISTICS OF THE READ, WRITE AND ERASE CYCLE FOR
PCM MATERIALS .............................................................................................. 60
FIGURE 37. PCM MEMORY CELL ....................................................................... 60
FIGURE 38. CROSS SECTION OF PCRAM CELL ................................................. 61
FIGURE 39. INTEL'S VIEW OF THE MEMORY-STORAGE HIERARCHY .......... 64
FIGURE 40. REDIS VIRTUAL MACHINE COUNT VS. MEMORY SIZE .......... 65
FIGURE 41. BASIC CELL DIAGRAM FOR FIELD SWITCHED MRAM ........ 66
FIGURE 42. FIELD SWITCHED ARRAY MRAM ARCHITECTURE............... 67
FIGURE 43. GYRFALCON AI ACCELERATOR WITH MRAM .................. 69
FIGURE 44. SPIN TRANSFER TORQUE OPERATION.............................. 71
FIGURE 45. STT MRAM CELL STRUCTURE........................................ 71
FIGURE 46. EVERSIPN STT MRAM DEVICE........................................ 72
FIGURE 47. PARALLEL TO ANTIPARALLEL SWITCHING ....................... 72
FIGURE 48. STT MRAM CURRENT OPERATION ..................................... 73
FIGURE 49. MULTI-BIT MRAM CELL READ OUT .................................. 74
FIGURE 50. A COMPARISON OF DRAM AND STT MRAM ..................... 75
FIGURE 51. STT MRAM CROSS SECTION ........................................ 75
FIGURE 52. IN PLANE (A) AND PERPENDICULAR (B) MAGNETIC TUNNEL CELLS............................................................... 76
FIGURE 53. COMPARISON OF MRAM, DRAM, FLASH AND HDD MEMORY DIMENSIONS............................................................. 76
FIGURE 54. STT MRAM EMBEDDED MEMORY....................................... 77
FIGURE 55. EXAMPLE MERAM DEVICE STRUCTURE............................ 78
FIGURE 56. CNT FABRIC .................................................................. 80
FIGURE 57. CNT BETWEEN SOURCE AND DRAIN .............................. 81
FIGURE 58. PFRAM 3-LAYER POLYMERIC MEMORY ............................ 82
FIGURE 59. FEFET TRANSISTOR ..................................................... 83
FIGURE 60. ORIGINAL SINGLE-PATTERNED FEATURES ...................... 85
FIGURE 61. CLAD THE SIDES OF THE ORIGINAL PATTERN .................. 85
FIGURE 62. REMOVE THE ORIGINAL PATTERN. THE REMAINING CLADDING IS A DOUBLED PATTERN ................................................... 85
FIGURE 63. CLAD THE SIDES OF THE DOUBLED PATTERN .................. 85
FIGURE 64. REMOVE THE DOUBLED PATTERN. THE REMAINING CLADDING IS THE QUADRUPLED PATTERN ................................................................. 86

FIGURE 65. NANOIMPRINT PROCESS ...................................................... 87

FIGURE 66. NANOIMPRINT DEPRESSIONS ........................................... 88

FIGURE 67. FLUID DISPENSE PROCESS ................................................ 88

FIGURE 68. LIGHT SPECTRUM ............................................................... 89

FIGURE 69. EUV SCANNING LITHOGRAPHIC EXPOSURE SYSTEM .......... 90

FIGURE 70. BIT DENSITY OF LARGEST MEMORIES PRESENTED AT IEEE RESEARCH CONFERENCES, 2001-2019 ......................................................... 96

FIGURE 71. FUTURE MEMORY/STORAGE HIERARCHY ......................... 98

FIGURE 72. MRAM MEMORY CELL ....................................................... 99

FIGURE 73. CROSS-SECTION OF AN MRAM DEVICE SHOWING DETAILS OF THE CMOS SUBSTRATE AND MAGNETIC LAYERS FABRICATED ON TOP OF THE SUBSTRATE ........................................................................ 100

FIGURE 74. MRAM MANUFACTURING PROCESS FLOW ....................... 100

FIGURE 75. KEY MRAM PROCESS EQUIPMENT ....................................... 101

FIGURE 76. APPLIED MATERIALS CMP SYSTEM .................................. 103

FIGURE 77. APPLIED MATERIALS ENDURA PLATFORM ....................... 104

FIGURE 78. CANON ANELVA EC7800 PVD EQUIPMENT ....................... 105

FIGURE 79. CANON ANELVA NC7900 PVD EQUIPMENT ....................... 106

FIGURE 80. LAM RESEARCH CLUSTER TOOLS ..................................... 106

FIGURE 81. SINGULUS TIMARIS II PVD CLUSTER TOOL PLATFORM .... 107

FIGURE 82. SINGULUS PVD CLUSTER TOOL PLATFORMS ..................... 107

FIGURE 83. TOKYO ELECTRON EXIM PVD CLUSTER TOOL PLATFORM 109

FIGURE 84. ULVAC MAGEST S200 MULTILAYER THIN FILM DEPOSITION SYSTEM ......................................................................................... 110

FIGURE 85. VEECO NEXUS IBD ION BEAM DEPOSITION SYSTEM ....... 110
FIGURE 86. A THREE GRID ION BEAM EXTRACTION SYSTEM ................. 111
FIGURE 87. SCHEMATIC OF MTJ ETCHING PROCESS ......................... 112
FIGURE 88. APPLIED MATERIALS CENTURA TOOL .......................... 112
FIGURE 89. APPLIED MATERIALS PRODUCER SYSTEM ..................... 113
FIGURE 90. CANON ANELVA NC8000 ION BEAM ETCH MACHINE ....... 113
FIGURE 91. HITACHI HIGH TECHNOLOGY E-600/800 NONVOLATILE ETCH SYSTEM ................................................................................................................ 114
FIGURE 92. LAM RESEARCH KIYO ION BEAM ETCHING CHAMBER ..... 115
FIGURE 93. OXFORD INSTRUMENTS IONFAB 300 IBE SYSTEM .......... 116
FIGURE 94. PLASMA THERM PINNACLE ION BEAM ETCH AND DEPOSITION SYSTEM ......................................................................................................... 116
FIGURE 95. ULVAC ULHITE NE-7800H NON-VOLATILE MATERIAL ETCHING TOOL .............................................................................................................. 117
FIGURE 96. VEECO NEXUS IBE-420I ION BEAM ETCHING SYSTEM .... 118
FIGURE 97. ASML DEEP UV PHOTOLITHOGRAPHY TOOL .................. 119
FIGURE 98. CANON LITHOGRAPHIC I-LINE STEPPER PRODUCT LINE .. 120
FIGURE 99. NIKON PHOTOLITHOGRAPHIC PRODUCT LINES ............. 121
FIGURE 100. TOKYO ELECTRON MRT300 MAGNETIC ANNEALING TOOL 121
FIGURE 101. ISI WLA 3000 WAFER LEVEL QUASI-STATIC TESTER ...... 122
FIGURE 102. HPROBE 3D HIGH MAGNETIC FIELD WAFER PROBE ...... 123
FIGURE 103. KEYSIGHT TECHNOLOGY NX5730A MRAM TEST PLATFORM 123
FIGURE 104. MICROSENSE POLAR KERR SYSTEM FOR PERPENDICULAR STT MRAM .................................................................................................................. 124
FIGURE 105. AFM EQUIPMENT ................................................................ 125
FIGURE 106. EQUIPMENT SPENDING BY REGION ............................. 127
FIGURE 107. NUMBER OF VOLUME FABS STARTING BY REGION (ALL PROBABILITIES, INCLUDING DISCRETES) .......................................................... 128
FIGURE 108. PROFITABILITY OF NAND FLASH MANUFACTURERS ...... 129
FIGURE 109. CHART OF BASELINE $/GB FOR STANDALONE MEMORY TECHNOLOGIES FROM 2017 THROUGH 2029 ........................................ 131
FIGURE 110. CHART OF ANNUAL BASELINE PETABYTE SHIPMENTS FOR STANDALONE MEMORY TECHNOLOGIES FROM 2017 THROUGH 2029 . 132
FIGURE 111. CHART OF BASELINE REVENUE ESTIMATES FOR MEMORY TECHNOLOGIES FROM 2018 THROUGH 2029 ($M) .................................. 134
FIGURE 112. CHART OF STANDALONE MRAM MEMORY WAFER ESTIMATES FOR THREE SCENARIOS COMPARED TO BASELINE CASE .................... 136
FIGURE 113. CHART OF EMBEDDED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE .............. 137
FIGURE 114. CHART OF COMBINED MRAM MEMORY WAFER ESTIMATES FOR HIGH AND LOW SCENARIOS COMPARED TO BASELINE CASE .......... 138
FIGURE 115. CHART OF HIGH, BASELINE AND LOW PETABYTE SHIPPING ESTIMATES FOR 3D XPOINT ............................................................ 140
FIGURE 116. CHART OF HIGH, BASELINE AND LOW REVENUE ESTIMATES FOR 3D XPOINT ............................................................................ 141
FIGURE 117. CHART OF COMBINED HIGH, BASELINE AND LOW PETABYTE SHIPPING ESTIMATES FOR EMERGING MEMORIES ..................... 143
FIGURE 118. CHART OF HIGH, BASELINE AND LOW STANDALONE REVENUE ESTIMATES FOR EMERGING MEMORIES ($M) ........................................ 145
FIGURE 119. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM ION BEAM ETCH EQUIPMENT FROM 2018 THROUGH 2029 . 148
FIGURE 120. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM PATTERNING EQUIPMENT FROM 2018 THROUGH 2029 ($M)150
FIGURE 121. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM PHYSICAL VAPOR EQUIPMENT FROM 2018 THROUGH 2029 ($M) ............................................................................... 152
FIGURE 122. CHART OF BASELINE SPENDING ESTIMATES FOR MRAM TEST AND OTHER EQUIPMENT FROM 2018 THROUGH 2029 ($M) .................... 154
FIGURE 123. CHART OF LOW, BASELINE AND HIGH SPENDING ESTIMATES FOR MRAM TEST AND OTHER EQUIPMENT FROM 2018 THROUGH 2029 ($M) ............................................................................................... 155

© 2019 Coughlin Associates and Objective Analysis
FIGURE 124. CHART OF BASELINE SPENDING ESTIMATES FOR MRAM EQUIPMENT FROM 2018 THROUGH 2029 ($M) .................................................. 156

FIGURE 125. CHART OF LOW, BASELINE AND HIGH TOTAL SPENDING ESTIMATES FOR MRAM EQUIPMENT FROM 2018 TO 2029 ($M) ........... 157
THE AUTHORS

Tom Coughlin, President, Coughlin Associates: Tom Coughlin has worked for over 37 years in the data storage industry. He has over 1000 publications and six patents. Tom is active with the IEEE, SMPTE, SNIA, and other professional organizations. Dr. Coughlin is an IEEE Fellow. He is co-chair of the iNEMI Mass Storage Technical Working Group, Education Chair for SNIA SSSI, he is President of IEEE-USA and a member of the IEEE Consultants Network of Silicon Valley. His publications include the Digital Storage Technology Newsletter, Media and Entertainment Storage Report and other reports. Tom is the author of Digital Storage in Consumer Electronics: The Essential Guide, now in its second edition with Springer. He has a regular Forbes.com blog called Storage Bytes and does a regular digital storage column for the IEEE Consumer Electronics Magazine.

He was the founder and organizer of the Storage Visions Conferences as well as the Creative Storage Conferences. He was general Chairman of the annual Flash Memory Summit for 10 years. Coughlin Associates provides market and technology analysis as well as data storage technical and market consulting. For more information go to www.tomcoughlin.com

Jim Handy, Objective Analysis: Jim Handy, a widely recognized semiconductor analyst, comes to Objective Analysis with over 30 years in the electronics industry including over 20 years as an industry analyst for Dataquest (now Gartner), Semico Research, and Objective Analysis. His background includes marketing and design positions at market-leading suppliers including Intel, National Semiconductor, and Infineon.

Mr. Handy is a member of the Mass Storage Technical Working Group of the International Electronics Manufacturing Initiative (iNEMI), and a member of the Storage Networking Industry Association (SNIA) Solid State Storage Initiative (SSSI). He is also a Leader in the Gerson Lehrman Group Councils of Advisors, serves on the Advisory Boards of the Flash Memory Summit and Storage Visions conferences. He is the author of three blogs covering SSDs (www.TheSSDguy.com), memory chips (www.TheMemoryGuy.com), and semiconductors for the investor (blogs.Forbes.com/JimHandy) and contributes to a number of other blogs.

A frequent presenter at trade shows, Mr. Handy is known for his widespread industry presence and volume of publication. He has written hundreds of articles for trade journals, Dataquest, Semico, and others, and is frequently interviewed and quoted in the electronics trade press and other media.

© 2019 Coughlin Associates and Objective Analysis
EXECUTIVE SUMMARY

Current memory technologies including flash memory (NAND and NOR), DRAM and SRAM are facing potential technology limits to their continued improvement. As a result, there are intense efforts to develop new memory technologies. Most of these new technologies utilize nonvolatile memory technologies and can be used for long-term storage or to provide a memory that does not lose information when power is not applied. This offers advantages for battery and ambient powered devices and also for energy savings in data centers.

The memories addressed in this report include PCM, ReRAM, FRAM, MRAM, STT MRAM and a variety of less mainstream technologies such as carbon nanotubes. Based upon the level of current development and the characteristics of these technologies, resistive RAM (ReRAM) may be a potential replacement for flash memory. However, flash memory has several generations of technologies that will be implemented before a replacement is required. Thus, this transition will not fully occur until the next decade at the earliest.

Micron and Intel's introduction of 3D XPoint Memory, a technology that has high endurance, performance much better than NAND, although somewhat slower than DRAM, and higher density than DRAM, could impact the need for DRAM. Intel introduced NVMe SSDs with its Optane technology (using 3D XPoint) in 2017 and began to ship NVDIMM Optane products in 2019, in support of its newest generation of server processors, the Second-Generation Intel Xeon Scalable Processors. 3D XPoint uses a type of phase change technology.

Magnetic RAM (MRAM) and spin transfer torque RAM (STT MRAM) will start to replace some NOR, SRAM and possibly DRAM within the next few years and probably before ReRAM replaces flash memory. The rate of development in STT MRAM and MRAM capabilities will result in gradually lower prices, and the attractiveness of replacing volatile memory with high speed and high endurance nonvolatile memory make these technologies very competitive, assuming that their volume increases to reduce production costs (and thus purchase prices).

Ferroelectric RAM (FRAM) and some ReRAM technologies have some niche applications and with the use of HfO FRAM the number of niche markets available for FRAM could increase in number.

Moving to a nonvolatile solid-state main memory and cache memory will reduce power usage directly as well as enable new power saving modes, provide faster recovery from power off and enable more stable computer architectures that retain their state even when power is off. Eventually spintronic technology, that uses spin rather than current for logic processes, could be used to make future microprocessors. Spin-based logic could enable very efficient in-memory processing. Several emerging memory technologies are also being used in neuromorphic computing experiments.
The use of a nonvolatile technology as an embedded memory combined with CMOS logic has great importance in the electronics industry. As a replacement for a multi-transistor SRAM, STT MRAM could reduce the number of transistors and thus provide a low cost, higher-density solution. A number of enterprise and consumer devices use MRAM, based on field switching, to act as an embedded cache memory, and this trend will continue.

The availability of STT MRAM has accelerated this trend and allows higher capacities. Because of the compatibility of MRAM and STT-RAM processes with conventional CMOS processes, these memories can be built directly on top of CMOS logic wafers. Flash memory doesn’t have the same compatibility with conventional CMOS. The power savings of nonvolatile and simpler MRAM and STT MRAM when compared with SRAM is significant. As MRAM $/GB costs approach those of SRAM, this replacement could cause significant market expansion.

We project that 3D XPoint Memory, with significant gigabyte shipments in 2020-2021, and with an assumed important price advantage versus DRAM will grow to a baseline level of 54.7EB (exabytes) of shipping capacity by 2029. 3D XPoint baseline revenues are projected to reach $16.1B by 2028.

It is projected that total MRAM and STT MRAM baseline annual shipping capacity will rise from an estimated 13.88TB in 2018 to 614PB in 2029. Standalone MRAM and STT-RAM baseline revenues are expected to increase from about $22M in 2018 to $3.8B by 2029. Much of this revenue gain will be at the expense of SRAM, NOR flash and some DRAM, although STT-RAM is developing its own special place in the pantheon of shipping memory technologies.

The demand for MRAM and STT-MRAM will drive demand for capital equipment to manufacture these devices. While MRAM and STT-MRAM can be built on standard CMOS circuits supplied by large semiconductor fabricators, MRAM and STT MRAM do require specialized fabrication equipment for the MRAM layers that is similar to or the same as that used in manufacturing the magnetic read sensors in hard disk drives.

The increasing demand for nonvolatile memory based upon MRAM and STT MRAM will cause total manufacturing equipment revenue used for making the MRAM devices to rise from an estimated $26M in 2018 to between $238M to $1.4B by 2029 with a baseline projected spending of $854M.
EMERGING MEMORIES RAMP UP

This report, jointly produced by Objective Analysis and Coughlin Associates, provides an exhaustive look at emerging memory technologies and their interaction with standard memories, both as discrete devices and in embedded applications (the memories within logic chips like ASICs and MCUs). The report provides a well of technical information, market dynamics, forecasts, and competitive analyses of the leading companies. Forecasts show how the markets will grow not only for the technologies themselves, but also for the capital equipment used to produce them. Read this to understand the competitive landscape and market drivers for these new memories, and to learn how to profit from tomorrow’s market.

Table of Contents (Top Level):

EXECUTIVE SUMMARY.................................................................17
INTRODUCTION:.............................................................................19
WHY EMERGING MEMORIES ARE POPULAR..............................23
HOW A NEW MEMORY LAYER IMPROVES COMPUTER PERFORMANCE ......31
UNDERSTANDING BIT SELECTORS.........................................38
RESISTIVE RAM, RERAM, RRAM, MEMRISTOR:......................46
FERROELECTRIC RAM, FERAM, FRAM:.....................................53
PHASE CHANGE MEMORY (PCM):...........................................58
INTEL/MICRON 3D CROSSPOINT MEMORY..........................62
MRAM (MAGNETIC RAM), STT MRAM (SPIN TRANSFER TORQUE MRAM)...............66
OTHER EMERGING MEMORY TYPES......................................79
LITHOGRAPHY:............................................................................84
3D MEMORY CIRCUIT DESIGN..............................................93
SUMMARY OF SOLID-STATE MEMORY & STORAGE TECHNOLOGIES ..........94
MRAM AND STT MRAM PROCESS EQUIPMENT......................99
PHASE CHANGE MANUFACTURING EQUIPMENT....................126
MEMORY IS DRIVING SEMICONDUCTOR CAPITAL SPENDING...........127
MARKET PROJECTIONS FOR MRAM, AND 3D XPOINT MEMORY ........128
ESTIMATES OF MRAM CAPITAL EQUIPMENT DEMAND.....................146
COMPANY INFORMATION:......................................................157

Order at: https://tomcoughlin.com/tech-papers/
or https://Objective-Analysis.com/reports/#Emerging

© 2019 Coughlin Associates and OBJECTIVE ANALYSIS, All Rights Reserved