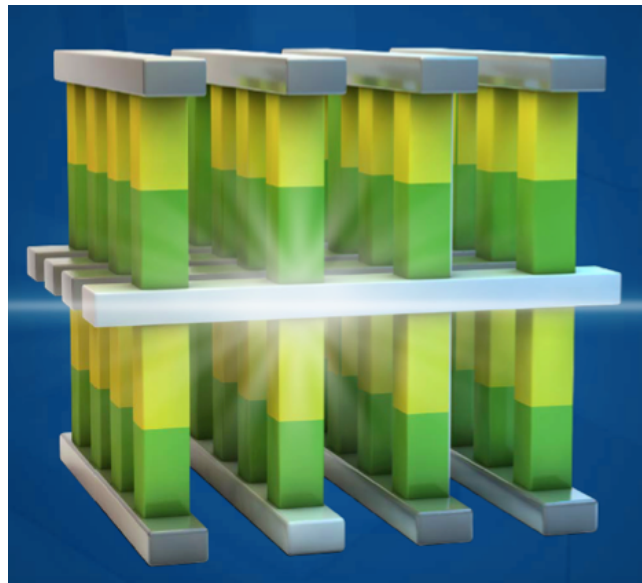
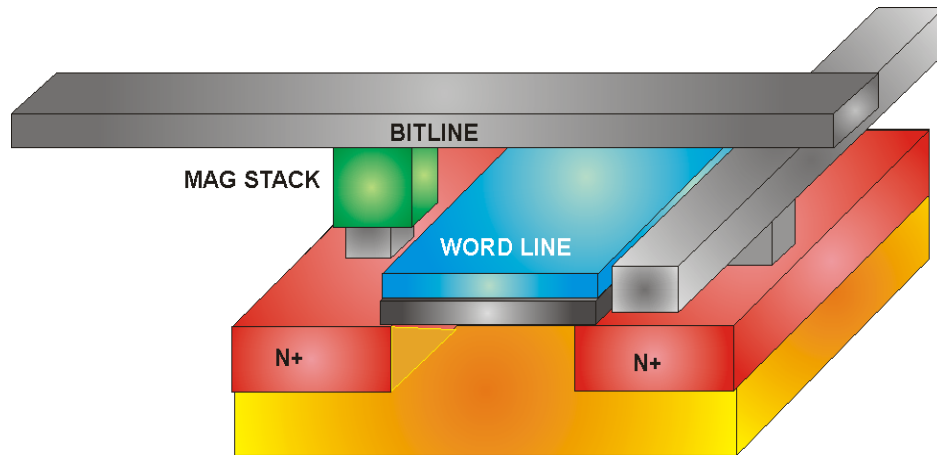


# EMERGING MEMORIES POISED TO EXPLODE

## *An Emerging Memory Report*



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**COUGHLIN ASSOCIATES**

**San Jose, California**

**July 2018**

**EMERGING MEMORIES POISED  
TO EXPLODE**  
*An Emerging Memory Report*

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Jim Handy, a widely recognized semiconductor analyst, comes to Objective Analysis with over 30 years in the electronics industry including over 20 years as an industry analyst for Dataquest (now Gartner), Semico Research, and Objective Analysis. His background includes marketing and design positions at market-leading suppliers including Intel, National Semiconductor, and Infineon.

Mr. Handy is a member of the Mass Storage Technical Working Group of the International Electronics Manufacturing Initiative (iNEMI), and a member of the Storage Networking Industry Association (SNIA) Solid State Storage Initiative (SSSI). He is also a Leader in the Gerson Lehrman Group Councils of Advisors, serves on the Advisory Boards of the Flash Memory Summit and Storage Visions conferences. He is the author of three blogs covering SSDs ([www.TheSSDguy.com](http://www.TheSSDguy.com)), memory chips ([www.TheMemoryGuy.com](http://www.TheMemoryGuy.com)), and semiconductors for the investor ([blogs.Forbes.com/JimHandy](http://blogs.Forbes.com/JimHandy)) and contributes to a number of other blogs.

A frequent presenter at trade shows, Mr. Handy is known for his widespread industry presence and volume of publication. He has written hundreds of articles for trade journals, Dataquest, Semico, and others, and is frequently interviewed and quoted in the electronics trade press and other media.

## **EXECUTIVE SUMMARY**

Current memory technologies including flash memory (NAND and NOR), DRAM and SRAM are facing potential technology limits to their continued improvement. As a result, there are intense efforts to develop new memory technologies. Most of these new technologies utilize nonvolatile memory technologies and can be used for long-term storage or to provide a memory that does not lose information when power is not applied. This offers advantages for battery and ambient powered devices and also for energy savings in data centers.

The memories addressed in this report include PCM, ReRAM, FRAM, MRAM, STT MRAM and a variety of less mainstream technologies such as carbon nanotubes. Based upon the level of current development and the characteristics of these technologies, resistive RAM (ReRAM) appears to be a potential replacement for flash memory. However, flash memory has several generations of technologies that will be implemented before a replacement is required. Thus, this transition will not fully occur until the next decade at the earliest.

Micron and Intel's introduction of 3D XPoint Memory, a technology that has high endurance, performance much better than NAND, although somewhat slower than DRAM, and higher density than DRAM; could impact the need for DRAM. Intel introduced NVMe SSDs with its Optane technology (using 3D XPoint) in 2017 and plans to ship NVDIMM Optane products in volume by 2019. 3D XPoint uses a type of phase change technology.

Magnetic RAM (MRAM) and spin tunnel torque RAM (STT MRAM) will start to replace some NOR, SRAM and possibly DRAM within the next few years and probably before ReRAM replaces flash memory. The rate of development in STT MRAM and MRAM capabilities will result in gradually lower prices, and the attractiveness of replacing volatile memory with high speed and high endurance nonvolatile memory make these technologies very competitive, assuming that their volume increases to reduce production costs (and thus purchase prices).

Ferroelectric RAM (FRAM) and some ReRAM technologies have some niche applications and with the use of HfO FRAM the number of niche markets available for FRAM could increase in number.

Moving to a nonvolatile solid-state main memory and cache memory will reduce power usage directly as well as enable new power saving modes, provide faster recovery from power off and enable more stable computer architectures that retain their state even when power is off. Eventually spintronic technology, that uses spin rather than current for logic processes, could be used to make future microprocessors. Spin-based logic could enable very efficient in-memory processing.

The use of a nonvolatile technology as an embedded memory combined with CMOS logic has great importance in the electronics industry. As a replacement for

a multi-transistor SRAM, STT MRAM could reduce the number of transistors and thus provide a low cost, higher-density solution. A number of enterprise and consumer devices use MRAM, based on field switching, to act as an embedded cache memory, and this trend will continue.

The availability of STT MRAM has accelerated this trend and allows higher capacities. Because of the compatibility of MRAM and STT-RAM processes with conventional CMOS processes, these memories can be built directly on top of CMOS logic wafers. Flash memory doesn't have the same compatibility with conventional CMOS. The power savings of nonvolatile and simpler MRAM and STT MRAM when compared with SRAM is significant. As MRAM \$/GB costs approach those of SRAM, this replacement could cause significant market expansion.

We project that 3D XPoint Memory, with significant gigabyte shipments in 2020-2021, and with an assumed significant price advantage versus DRAM will grow to a baseline level of 30PB (petabytes) of shipping capacity by 2028. 3D XPoint revenues are projected to reach \$3.0 B by 2028.

It is projected that MRAM and STT MRAM baseline annual shipping capacity will rise from an estimated...

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